In the Claims:

1. (Previously presented) An integrated circuit device, comprising:

a delay circuit that is configured to delay a clock signal and is further configured to generate an output data signal in response to the delayed clock signal and an input data signal, the delay circuit comprising:

a memory unit that is configured to store delay information therein;

a delay buffer that is coupled to the memory unit and is configured to generate the delayed clock signal at an output terminal thereof in response to the delay information and the clock signal received at an input terminal thereof; and

a receiver circuit that is configured to store the input data signal and to generate the output data signal in response to the delayed clock signal and the stored input data signal;

an input terminal that is coupled to both the receiver circuit and the memory unit and is configured to receive the input data signal and the delay information therethrough; and

a plurality of devices that are configured to respectively receive the output data signal in response to the clock signal.

2. (Canceled)

3. (Previously presented) The integrated circuit device of Claim1, wherein the delay buffer comprises:

a plurality of buffers; and

a plurality of switches that are respectively operable to connect selected ones of the plurality of buffers in series between the input terminal and the output terminal of the delay buffer.

4. (Original) The integrated circuit device of Claim 3, wherein the delay circuit further comprises:

a demultiplexer circuit that couples the memory unit to the delay buffer and is configured to generate a plurality of switch control signals, respective ones of the plurality of switches being responsive to the respective ones of the plurality of switch control signals.

5. (Canceled)

6. (Canceled)

7. (Original) The integrated circuit device of Claim 1, wherein the plurality of devices comprises memory devices.

8. (Original) The integrated circuit device of Claim 1, further comprising:

a clock generation circuit that is configured to generate the clock signal in response to an input clock signal.

9. (Original) The integrated circuit device of Claim 8, wherein the clock generation circuit is a phase locked loop circuit.

10. (Original) The integrated circuit device of Claim 8, respective ones of the plurality of devices have different respective delays associated therewith with respect to receiving the output data signal.

11. (Original) An integrated circuit device, comprising:

a delay circuit that is configured to receive an input data signal in response to a clock signal and is further configured to generate an output data signal by delaying the input data signal, the delay circuit comprising:~~; and~~

a memory unit that is configured to store delay information therein;

a delay buffer that is coupled to the memory unit and is configured to generate the output data signal at an output terminal thereof in response to the delay information and the input data signal received at an input terminal thereof; and

a receiver circuit that is configured to store the input data signal in response to the clock signal;

an input terminal that is coupled to both the receiver circuit and the memory unit and is configured to receive the input data signal and the delay information therethrough; and

a plurality of devices that are configured to respectively receive the output data signal in response to the clock signal.

12. (Canceled)

13. (Currently amended) The integrated circuit device of Claim ~~12~~ 11, wherein the delay buffer comprises:

a plurality of buffers; and

a plurality of switches that are respectively operable to connect selected ones of the plurality of buffers in series between the input terminal and the output terminal of the delay buffer.

14. (Original) The integrated circuit device of Claim 13, wherein the delay circuit further comprises:

a demultiplexer circuit that couples the memory unit to the delay buffer and is configured to generate a plurality of switch control signals, respective ones of the plurality of switches being responsive to the respective ones of the plurality of switch control signals.

15. (Canceled)

16. (Canceled)

17. (Original) The integrated circuit device of Claim 11, wherein the plurality of devices comprises memory devices.

18. (Original) The integrated circuit device of Claim 11, further comprising:

a clock generation circuit that is configured to generate the clock signal in response to an input clock signal.

19. (Original) The integrated circuit device of Claim 18, wherein the clock generation circuit is a phase locked loop circuit.

20 - 31. (Canceled)